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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/660,814	09/12/2003	Satwant Singh	M-15198 US	7052

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Jon W. Hallman
MacPHERSON KWOK CHEN & HEID LLP
Suite 226
1762 Technology Drive
San Jose, CA 95110

EXAMINER	
CHANG, DANIEL D	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 02/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/660,814	SINGH ET AL.	
	Examiner	Art Unit	
	Daniel D. Chang	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 January 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13,17-20 and 32-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,17-20 and 32-34* is/are rejected.

7)☒ Claim(s) *10-13 and 35-37* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/9/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Election/Restrictions

Applicant's election without traverse of Group I, Claims 1-13, 17-20, and 32-37 in the reply filed on January 28, 2005 is acknowledged.

Claim Objections

Claim 10 is objected to because of the following: on lines 2 and 4, the recitation, "may" and "may be" should be deleted or changed to better form since it fails to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2, 4-9, 17-20, and 32-34 are rejected under 35 U.S.C. 102(b) as being anticipated by Lien et al. (US 6,211,697 B1, hereinafter Lien).

Regarding claim 1, Lien discloses an application specific integrated circuit (ASIC) (24 in Fig. 1; col. 2, lines 53) conversion of a programmable logic device (PLD) (22 in fig. 1; col. 2, lines 7+), wherein the programmable logic device comprises a plurality of PLD logic blocks and a PLD routing structure (see Figs. 2 and 3) operable to couple logical inputs to each PLD logic block, comprising:

a plurality of ASIC logic blocks (40 in Fig. 4) corresponding on a one-to-one basis with the plurality of PLD logic blocks (40 in Fig. 3); and

an ASIC routing structure (Fig. 4) configured to couple logical inputs to each ASIC logic block, wherein the coupling provided by the ASIC routing structure is the same (col. 4, lines 53+; col. 7, lines 3+; col. 7, lines 53+) as that provided by the PLD routing structure (Fig. 3).

Regarding claim 2, Lien discloses that the PLD logic blocks and the ASIC logic blocks are lookup table (LUT)-based logic blocks (see Figs. 5 and 6).

Regarding claim 4, Lien discloses that the ASIC includes a plurality of metal layers (col. 7, lines 24+); wherein at least a first metal layer and a second metal layer in the plurality are coupled by vias (130, 132, 134 in Fig. 4; col. 7, lines 24+) each selected so as to provide either a logic high or a logic low value (col. 8, lines 23+) to the plurality of ASIC logic blocks to provide the same truth tables as used in the PLD logic blocks (col. 7, lines 53+).

Regarding claim 5, Lien discloses that the ASIC includes at least one metal layer (col. 7, lines 24+), wherein traces formed in the metal layer are customized to provide the same truth tables for the ASIC logic blocks as are used in the PLD logic blocks (col. 7, lines 53+).

Regarding claim 6, Lien discloses that only the first and second metal layers are coupled by vias (130, 132, 134 in Fig. 4; col. 7, lines 24+) selected so as to provide either a logic high or a logic low value (col. 8, lines 23+) to the plurality of ASIC logic blocks to thereby provide the same truth tables as in the PLD logic blocks (col. 7, lines 53+).

Regarding claim 7, Lien discloses that the first metal layer includes traces carrying voltage levels VCC and VSS, and wherein the vias (130, 132, 134 in Fig. 4; col. 7, lines 24+) are

selected to couple to VCC to provide a logic high value and to couple to VSS to provide a logic low value (col. 8, lines 23+).

Regarding claim 8, Lien discloses that the ASIC includes a plurality of metal layers, and wherein at least a first metal layer and a second metal layer in the plurality are coupled by vias (130, 132, 134 in Fig. 4; col. 7, lines 24+) each selected so that the coupling provided by the ASIC routing structure routing structure is the same as that provided by the PLD routing structure (col. 4, lines 53+; col. 7, lines 3+).

Regarding claim 9, Lien discloses that the PLD routing structure is a buffered, segmented routing structure, each buffered PLD routing segment corresponding to an ASIC buffered routing segment, and wherein the vias (130, 132, 134 in Fig. 4; col. 7, lines 24+) are each selected so that the coupling provided by the ASIC routing structure is the same as that provided by the PLD routing structure on a segment-by-segment basis (col. 4, lines 53+; col. 7, lines 3+).

Claims 17-20 are essentially the same in scope as apparatus claims 1, 2, and 4-9, and are rejected similarly.

Regarding claim 32, Lien discloses an application specific integrated circuit (ASIC) (24 in Fig. 1; col. 2, lines 53) comprising:

a plurality of logic blocks corresponding to programmable logic blocks of a programmable logic device (PLD) (22 in fig. 1; col. 2, lines 7+); and

a routing structure (Fig. 4) corresponding to the programmable routing structure of the PLD (Fig. 3) but having permanently formed connections therein, the ASIC routing structure adapted to produce a signal propagation delay that matches (col. 12, 39+, 51+) substantially the signal propagation delay in the corresponding PLD programmable routing structure.

Regarding claim 33, Lien discloses that the permanently formed connections of the ASIC routing structure include selectively formed vias (130, 132, 134 in Fig. 4; col. 7, lines 24+) between conductive layers to provide a desired route through the routing structure.

Regarding claim 34, Lien discloses that the permanently formed connections of the ASIC routing structure include selectively formed vias (130, 132, 134 in Fig. 4; col. 7, lines 24+) between conductive layers to produce a desired capacitive load (it is inherent that any conductor such as a signal line have a capacitance) on the routing structure.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lien.

The teachings of Lien have been discussed above. Lien does not disclose that the ASIC logic blocks are programmable AND array-based logic blocks.

However, it is well known in the art that programmable AND array-based logic blocks will work similarly with hard gate array. It would have been obvious at the time the invention was made to a person having ordinary skill in the art to substitute the hard array of Lien with programmable AND array-based logic blocks because it is an obvious matter of substitution of equivalence.

Allowable Subject Matter

Claims 10-13 and 35-37 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel D. Chang whose telephone number is (571) 272-1801. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael J. Tokar can be reached on (571) 272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Daniel D. Chang
Primary Examiner
Art Unit 2819

dc

DANIEL CHANG
PRIMARY EXAMINER